

WHAT IS CLAIMED IS:

- 1 1. A wafer for use in a chip device comprising:
  - 2 a. a non-passivated wafer;
  - 3 b. a first titanium layer;
  - 4 c. a first copper layer above the first titanium layer;
  - 5 d. a second titanium layer above the first copper layer; and
  - 6 e. a second copper layer above the second titanium layer.

- 1 2. A wafer in accordance with claim 1 further comprising a plurality  
2 of solder bumps.

- 1 3. A chip device comprising a wafer, the wafer comprising:
  - 2 a. a non-passivated wafer;
  - 3 b. a first titanium layer;
  - 4 c. a first copper layer above the first titanium layer;
  - 5 d. a second titanium layer above the first copper layer; and
  - 6 e. a second copper layer above the second titanium layer.

- 1 4. A method of preparing a wafer for use in a chip device, the method  
2 comprising:
  - 3 providing a non-passivated wafer;
  - 4 depositing a first titanium layer on the non-passivated wafer;
  - 5 depositing a first copper layer on the first titanium layer;
  - 6 depositing a second titanium layer on the first copper layer; and
  - 7 depositing a second copper layer on the second titanium layer.

- 1 5. A method of making a bumped wafer, the method comprising:
  - 2 providing a non-passivated die;
  - 3 alternately sputtering a first titanium layer, a first copper layer, a second  
4 titanium layer and a second copper layer onto the die;
  - 5 depositing photo resist material onto the second copper layer;

6 etching isolation areas thereby removing the photo resist material, the  
7 second copper layer, the second titanium layer and the first copper layer at the isolation  
8 areas;  
9 depositing photo resist material to define bump locations;  
10 etching bump locations thereby removing the second copper layer and the  
11 second titanium layer at the bump locations  
12 depositing under-bump material at the bump locations;  
13 depositing solder on the under-bump material;  
14 removing the photo resist material  
15 etching away the second titanium layer at the isolation locations;  
16 etching away the remaining second copper layer; and  
17 reflowing the solder.